1. SPI Protocol

This document reflects the Novotechnik sensor protocol implementation of the standard SPI protocol. A basic knowledge of the SPI Bus is required for a proper understanding of this document.

1.1 Bus Topology

SPI communication with only 1 slave:

```
SPI Master    SCLK  MOSI  MISO  SS
             SPI    MISO  Slave
```

SPI communication with more than 1 slave:

```
SPI Master    SCLK  MOSI  MISO  SS
             SPI    MISO  Slave
             SCLK  MOSI  SPI  Slave
             SCLK  MOSI  SPI  Slave
             SCLK  MOSI  SPI  Slave
```
1.2 Electrical Characteristics
The serial protocol of Novotechnik Single turn sensors is a three wires protocol (/SS, SCLK, MOSI-MISO).
- /SS pin is a 5V tolerant digital input
- SCLK pin is a 5V tolerant digital input
- MOSI-MISO pin (both lines are combined in the sensor to form one data line) is a 5V tolerant open drain digital input/output

Resistor values

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V μCtrl w/o O.D. w/o 3.3 V</td>
<td>5 V</td>
<td>5 V</td>
<td>5 V</td>
<td>100</td>
<td>1000</td>
<td>20000</td>
<td>1000</td>
<td>20000</td>
<td>BS 170</td>
</tr>
<tr>
<td>5 V μCtrl w/o O.D. w 3.3 V</td>
<td>5 V</td>
<td>3.3 V</td>
<td>5 V</td>
<td>150</td>
<td>1000</td>
<td>-</td>
<td>1000</td>
<td>20000</td>
<td>BS 170</td>
</tr>
<tr>
<td>3.3 V μCtrl w/o O.D. **</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>5 V</td>
<td>150</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>BS 170</td>
</tr>
<tr>
<td>5 V μCtrl w O.D. w/o 3.3 V**</td>
<td>5 V</td>
<td>5 V</td>
<td>5 V</td>
<td>100</td>
<td>1000</td>
<td>20000</td>
<td>1000</td>
<td>20000</td>
<td>BS 170</td>
</tr>
<tr>
<td>3.3 V μCtrl w O.D.</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>5 V</td>
<td>150</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>BS 170</td>
</tr>
</tbody>
</table>

*) μCtrl w O.D.: Micro Controller with open-drain capability (e.g. NEC V850 series)
**) μCtrl w/o O.D.: Micro Controller without open-drain capability (e.g. TI TMS320 series, AMTEL AVR)

1.3 SPI Mode
Clock phase CPHA = 1 even clock changes are used to sample the data
Clock polarity CPOL = 0 active high clock
The positive going edge shifts a bit to the slave’s output stage and the negative going edge samples the bit at the master’s input stage.

1.4 MOSI (Master Out, Slave In)
The master sends a command to the slave to get the angle information.

1.5 MISO (Master In, Slave Out)
The MISO of the slave is an open-collector stage. Due to the capacitive load a > 1k Ohmpull-up is used for the recessive high level.

1.6 /SS Slave Select
The /SS pin enables a frame transfer (if CPHA = 1). It allows a re-synchronisation between slave and master in case of communication error.

1.7 Master Start-up
/SS, SCLK, MISO can be undefined during the master start-up as long as the slave is re-synchronized before the first frame transfer.

1.8 Slave Start-up
The slave start-up (after power-up or an internal failure) takes 10 ms. Within this time /SS and SCLK is ignored by the slave. The first frame can therefore be sent after 10 ms.
MISO is high-impedant until the slave is selected by its /SS input.
The sensor will cope with any signal from the master while starting up.
1.9 Timing
To synchronize communication, the master deactivates /SS high for at least \( t_5 \) (300 \( \mu \)s).

In this case, the slave will be ready to receive a new frame.

The master can re-synchronize at any time, even in the middle of a byte transfer.

Note: Any time shorter than \( t_5 \) leads to an undefined frame state, because slave may or may not have seen /SS inactive.

![Timing Diagram](image)

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### Timing

<table>
<thead>
<tr>
<th>Timing</th>
<th>Min</th>
<th>Max</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_1 )</td>
<td>2.3 ( \mu )s</td>
<td>-</td>
<td>No capacitive load on MISO. ( t_1 ) is the minimum clock period for any bits within a byte</td>
</tr>
<tr>
<td>( t_2 )</td>
<td>12.5 ( \mu )s</td>
<td>-</td>
<td>( t_2 ) is the minimum time between any other byte</td>
</tr>
<tr>
<td>( t_4 )</td>
<td>2.3 ( \mu )s</td>
<td>-</td>
<td>Time between last clock and /SS = high</td>
</tr>
<tr>
<td>( t_5 )</td>
<td>300 ( \mu )s</td>
<td>-</td>
<td>Minimum /SS = high time where it is guaranteed that a frame reconstructions will be started</td>
</tr>
<tr>
<td>( t_6 )</td>
<td>0 ( \mu )s</td>
<td>-</td>
<td>Minimum /SS = high time where it is guaranteed that no frame reconstructions will be started</td>
</tr>
<tr>
<td>( t_7 )</td>
<td>2.3 ( \mu )s</td>
<td>-</td>
<td>Time ( t_6 ) defines the minimum time between /SS = low and the first clock edge</td>
</tr>
<tr>
<td>( t_8 )</td>
<td>15 ( \mu )s</td>
<td>-</td>
<td>( t_8 ) is the minimum time between start byte and byte 0</td>
</tr>
<tr>
<td>( t_9 )</td>
<td>0 ( \mu )s</td>
<td>-</td>
<td>Minimum time where SS is deactivated between a ID byte and a start byte</td>
</tr>
<tr>
<td>t start up</td>
<td>-</td>
<td>&lt;1 ( \mu )s</td>
<td>Maximum time between /SS = high and MISO Bus High-Impedance</td>
</tr>
</tbody>
</table>

1.10 Slave Reset
On internal soft failures the slave will reset after 1 s, or after an (error) frame is sent.
On internal hard failures the slave will reset itself. In that case the serial protocol will not come up.

The serial protocol link is enable only after the completion of the first synchronisation (the master deactivates /SS for at least \( t_5 \)).

1.11 Frame Layer
Before each transmission of a data frame, the master should send a byte AAh to enable a frame transfer.

The latch point for the angle measurement is at the last clock of the first data frame byte.

![Timing Diagram - dual slave communication](image)
1.12 Data Frame Structure
A data frame consists of 10 bytes
- 2 start bytes (AAh followed by FFh)
- 2 data bytes (Data 16 – most significant byte first)
- 2 inverted data bytes (/Data16 - most significant byte first)
- 4 all-high bytes
The master should send AAh followed by nine bytes FFh.
The slave will answer with two bytes FFh followed by four data bytes and four bytes FFh.

1.13 Timing
There are no timing limits for frames: a frame transmission could be initiated at any time.
There is no inter-frame time defined.

1.14 Data Structure
The Data16 could be a valid angle or an error condition. The two meanings are distinguished by the LSB.


<table>
<thead>
<tr>
<th>Most Significant Byte</th>
<th>Less Significant Byte</th>
</tr>
</thead>
<tbody>
<tr>
<td>A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0</td>
<td>0 1</td>
</tr>
</tbody>
</table>

Data 16: Error

<table>
<thead>
<tr>
<th>Most Significant Byte</th>
<th>Less Significant Byte</th>
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<tbody>
<tr>
<td>E15 E14 E13 E12 E11 E10 E9 E8 E7 E6 E5 E4 E3 E2 E1 E0</td>
<td></td>
</tr>
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</table>

1.15 Angle Calculation
All communication timing is independent (asynchronous) of the angle data processing.
The angle is calculated continuously by the slave every 350 µs.
The last angle calculated is hold to be read by the master at any time.
Note: Only valid angles are transferred by the slave, because any internal failure of the slave will lead to a soft reset.

1.16 Error Handling
In case of any errors listed in chapter 1.12, the serial protocol will be initialized and the error condition can be read by the master. The slave will perform a soft reset once the error frame is sent.
In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error,...) the slave’s serial protocol is not initialized. The MOSI/MISO pin will stay high (no error frame is sent).

1.17 Document Changes

<table>
<thead>
<tr>
<th>Revision</th>
<th>Changes</th>
<th>Date</th>
<th>Who</th>
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<tr>
<td>V00</td>
<td>First edition</td>
<td>23.04.19</td>
<td>VM/mm</td>
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<tr>
<td>V01</td>
<td>1.2 Resistor value R3 and R5: 20000 Ohm instead of 20 Ohm</td>
<td>02.12.20</td>
<td>VM/mm</td>
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